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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
BP3012

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on **April 19, 2006** Signature **/Bruce E. Garlick, 36,520/** Typed or printed name **Bruce E. Garlick, 36,520**	Application Number **10/791,945**	Filed **3/12/2004**
	First Named Inventor **Li Fung Chang**	
	Art Unit **2631**	Examiner **Juan A. Torres**

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
        Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

☑ attorney or agent of record. **36,520**
Registration number

☐ attorney or agent acting under 37 CFR 1.34.

Registration number if acting under 37 CFR 1.34 _____

/Bruce E. Garlick, 36,520/
Signature

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Telephone number

April 19, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required.
Submit multiple forms if more than one signature is required, see below*.

☐ *Total of __1__ forms are submitted.

In the Application of:
Li Fung Chang

Serial No.: 10/791,945

For: EDGE INCREMENTAL
REDUNDANCY SUPPORT IN A
CELLULAR WIRELESS TERMINAL

§ Group Art Unit: 2631
§ Examiner: Juan A. Torres
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§ Filed: March 3, 2004
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REQUEST FOR REVIEW OF FINAL OFFICE ACTION

The Final Office Action mailed December 19, 2005 rejected claims 1 and 16 (among others) under 35 U.S.C. 102(b) as being anticipated by Pukkila (US 20010017904 A1). The Office Action rejected claims 1 and 16 (among others) under 35 U.S.C. 102(e) as being anticipated by Parolari (US 20040081248 A1). Applicants disagree with these rejections and

5   request review.

Claims 1 is not anticipated under 35 U.S.C. 102(b) by Pukkila

Independent claim 1 is directed to a "method for performing Incremental Redundancy (IR) operations in a wireless receiver." This method includes (1) receiving an analog signal corresponding to a data block; (2) sampling the analog signal to produce samples; (3) equalizing the

10   samples to produce soft decision bits of the data block; (4) configuring, by a system processor of the wireless receiver, a plurality of IR processing module registers; (5) initiating, by the system processor of the wireless receiver, operation of an IR processing module of the wireless receiver; (6) accessing, by the IR processing module, the plurality of IR processing module registers; and (7) performing, by the IR processing module, IR operations on the soft decision bits of the data block in

15   an attempt to correctly decode the data block.

The Office Action equates block 205' of FIG. 2 and blocks 305-318 of FIG. 3 of Pukkila with "configuring, by a system processor of the wireless receiver, a plurality of IR processing module registers." As Pukkila describes at paragraph 25, last sentence, block 205' is a "turbo equalizer." Block 205' of FIG. 2 of Pukkila performs equalization, deinterleaving, decoding, and

20   reinterleaving operations. Block 205'. Block 205' of FIG. 2 of Pukkila and the associated operations of FIG. 3 cannot be equated the operations of claim 1 performed by a system processor. Blocks 305-318 do not disclose, suggest, or teach "configuring, by a system processor of the wireless receiver, a plurality of IR processing module registers."

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The Office Action equates block 205' of FIG. 2 and blocks 305-318 of FIG. 3 of Pukkila with "initiating, by the system processor of the wireless receiver, operation of an IR processing module of the wireless receiver." As Pukkila describes at paragraph 25, last sentence, block 205' is a "turbo equalizer." Block 205' of FIG. 2 of Pukkila performs equalization, deinterleaving, decoding, and reinterleaving operations. Block 205' of FIG. 2 of Pukkila cannot be equated to a system processor. Further, blocks 305-318 do not disclose, suggest, or teach "initiating, by the system processor of the wireless receiver, operation of an IR processing module of the wireless receiver."

The Office Action equates block 205' of FIG. 2 and blocks 305-318 of FIG. 3 of Pukkila with "accessing, by the IR processing module, the plurality of IR processing module registers." As Pukkila describes at paragraph 25, last sentence, block 205' is a "turbo equalizer." Block 205' of FIG. 2 of Pukkila performs equalization, deinterleaving, decoding, and reinterleaving operations. Block 205' of FIG. 2 of Pukkila cannot be equated with an IR processing module. Further, blocks 305-318 do not disclose, suggest, or teach "accessing, by the IR processing module, the plurality of IR processing module registers."

The Office Action equates block 205' of FIG. 2 and blocks 305-318 of FIG. 3 of Pukkila with "performing, by the IR processing module, IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block." As Pukkila describes at paragraph 25, last sentence, block 205' is a "turbo equalizer." Block 205' of FIG. 2 of Pukkila performs equalization, deinterleaving, decoding, and reinterleaving operations. Block 205' of FIG. 2 of Pukkila cannot be equated with an IR processing module. Further, blocks 305-318 do not disclose, suggest, or teach "performing, by the IR processing module, IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block."

Claims 16 is not anticipated under 35 U.S.C. 102(b) by Pukkila

Independent claim 16 is directed to a "system for implementing Incremental Redundancy (IR) operations in a wireless receiver." This system includes: (1) a baseband processor that is operable to receive analog signals corresponding to a data block and to produce samples of the analog signals; (2) an equalizer that is operable to receive the samples from the baseband processor, to equalize the samples, and to produce soft decision bits of the data block; (3) a system processor that is operable to receive the soft decision bits of the data block; (4) a plurality of IR processing module registers communicatively coupled to the system processor; (5) an IR processing module

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communicatively coupled to the system processor and to the plurality of IR processing module registers; (6) wherein the system processor is operable to configure the plurality of IR processing module registers and to initiate operation of the IR processing module of the wireless receiver; and (7) wherein the IR processing module is operable to access the plurality of IR processing module registers, to receive the soft decision bits of the data block, and to perform IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block.

The Office Action equates block 203 of Pukkila (Ampl., A/D) with the baseband processor of claim 16. Block 203 of Pukkila is a combined amplifier and analog to digital converter. A combined amplifier and analog to digital converter is simply not equivalent to a baseband processor. A baseband processor, in addition to performing amplification and analog-to-digital conversion operations, is capable of performing significant other baseband processing operations, as is described in the specification of the present application. Thus, the combined amplifier and analog to digital converter of Pukkila block 203 does not identically set forth the baseband processor of claim 16. For this reason, Pukkila does not anticipate claim 16.

The Office Action equates four elements of claim 16 with block 205' of Pukkila. Firstly, the Office Action equates the equalizer of claim 16 with block 205 (of block 205') of FIG. 2 of Pukkila. Secondly, the Office Action equates the plurality of IR processing module registers with block 205' of FIG. 2 (and operations of FIG. 3) of Pukkila. Thirdly, the Office Action equates the system processor with block 205' of FIG. 2 (and operations of FIG. 3) of Pukkila. Fourthly, the Office Action equates the IR processing module with block 205' of FIG. 2 (and operations of FIG. 3) of Pukkila. Equating block 205' with multiple claim elements is impermissible in making an anticipation rejection. Each teaching of a prior art reference can only be used to meet one claim element. Because block 205' is cited against multiple elements of claim 16, Pukkila does not anticipate claim 16.

Block 205' of FIG. 2 of Pukkila cannot be equated to the system processor, the plurality of IR processing module registers, or the IR processing module of claim 16. As Pukkila describes at paragraph 25, last sentence, block 205' is a "turbo equalizer." Block 205' of FIG. 2 of Pukkila performs equalization, deinterleaving, decoding, and reinterleaving operations. Block 205' of FIG. 2 and the related operations of FIG. 3 of Pukkila do not identically set forth the "system processor that is operable to receive the soft decision bits and to initiate IR operations" of claim 16. Block 205' of FIG. 2 and the related operations of FIG. 3 of Pukkila do not identically set forth the

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"plurality of IR processing module registers communicatively coupled to the system processor" of claim 16. Block 205' of FIG. 2 and the related operations of FIG. 3 of Pukkila do not identically set forth the "IR processing module operably coupled to the system processor that is operable to receive the soft decision bits and to perform IR operations on the soft decision bits" of claim 16. Thus,

5   Pukkila does not disclose the system processor, the plurality of IR processing module registers, or the IR processing module of claim 16. For each of these reasons, Pukkila does not anticipate claim 16.

Pukkila further fails to describe the interaction among the elements of claim 16. Pukkila does not describe how "the system processor is operable to configure the plurality of IR processing

10   module registers and to initiate operation of the IR processing module of the wireless receiver." Further, Pukkila does not described how "the IR processing module is operable to access the plurality of IR processing module registers, to receive the soft decision bits of the data block, and to perform IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block." For these additional reasons, Pukkila does not anticipate claim 16.

15   **Claims 1 and 16 are not anticipated under 35 U.S.C. 102(e) by Parolari**

The Office Action cites FIG. 5 and related text of Parolari as anticipating claims 1 and 16. FIG. 5 of Paraolari illustrates a control processor, an equalizer, and an incremental redundancy buffer, among other elements. At best Paraolari discloses the system processor and equalizer of claim 16 and their related operations of claim 1. Paraolari does not disclose an IR

20   processing module and a baseband processor that are distinct from other system components as required by claim 16. Further, claim 16 requires that "wherein the system processor is operable to configure the plurality of IR processing module registers and to initiate operation of the IR processing module of the wireless receiver; and wherein the IR processing module is operable to access the plurality of IR processing module registers, to receive the soft decision bits of the data

25   block, and to perform IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block." These elements of claim 16 and similar operations of claim 1 are not even contemplated by Parolari, much less disclosed or taught by the reference.

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